IN THE SPECIFICATION

Page 1, line 4, please replace the paragraph beginning "In current electronic circuits" with the following:

In current electronic circuits, a very high integration density of electrical functions on a small volume or small area is desired. This ~~is~~ may be achieved, for example, ~~in that functions are designed in~~using a three-dimensional circuit arrangement in a multilayer process. In the case of integrated electrical resonant circuits which are produced using planar technology, for example using multilayer laminate processes and Low Temperature Cofire Ceramic (LTCC) processes, capacitors and coils having metal structures are incorporated in the multilayer substrate. The integration of capacitors in such multilayer circuits is nevertheless only possible to a limited extent. This is because many multilayer processes exhibit fluctuations in the layer thickness, with the statistical fluctuation in layer thicknesses often being up to 10%, and since the capacitance of a plate capacitor changes as a function of the layer thickness of the dielectric layer between the electrodes an integrated capacitor would also fluctuate by 10% of its capacitance. This leads to corresponding fluctuations in the electrical response of the integrated functions, and the frequency of a filter designed with integrated coils and capacitors cannot be kept constant in accordance with the specifications. Nowadays, therefore, in multilayer stacks many components are still soldered onto the circuit as external components, with these being checked for their set value prior to assembly. The capacitors are sorted in terms of their capacitance and exhibit variations of typically less than 5%. These external components limit the miniaturization and entail higher costs on

account of the assembly. In addition, the soldering process used for these external components in the assembly has a higher error rate than would be the case for integrated capacitors, and thus often leads to failure of the product.

Page 2, line 5, replace the paragraph beginning "The circuit of Fig. 1(a)" with the following:

The circuit of FIG. 1(a) shows a grounded series resonant circuit, consisting of a coil L1 and a grounded capacitor C1. At the resonant frequency of the resonant circuit, a high frequency signal ~~moving from point 1 to point 2~~ is reflected, since the resonant circuit at this frequency acts as a short circuit.

Page 2, line 18, please delete in its entirely the paragraph beginning "This object is achieved".

Page 2, line 30, replace the pargraph beginning "According to the invention" with the following:

According to the invention, in a multilayer stack having a metallization structure as defined above it is also provided that this metallization layer is arranged on a dielectric layer, the dielectric constant ε_{medium} of which is greater than the dielectric constant .epsilon. of the surrounding dielectric layers. "Surrounding layers" means the layers adjoining the layer having the dielectric constant ε_{medium}. The dielectric constant of such

surrounding layers is represented by ε and the thickness of such surrounding layers is represented by d_ε. It has been found that, in such an arrangement, variations in the layer thickness of the dielectric layer having the dielectric constant ε_{medium} only very slightly affect the transmission characteristic or the shift in resonant frequency. If, specifically within the dielectric layer, the layer thickness decreases, the capacitance of the capacitor is increased. At the same time, the metal line is located closer to the ground electrode. This line acts as a coil. At the ground electrode, mirror currents are induced which lower the inductance of the line. The closer the line is to the ground electrode, the lower the inductance of the line. The product of capacitance and inductance thus remains approximately constant and hence so does the resonant frequency

$$f = \frac{1}{2\pi\sqrt{L \cdot C}}$$

of the circuit. Inversely, when the layer thickness increases the capacitance of the capacitor becomes smaller, while the inductance of the line becomes greater. As a result the product LC again remains approximately constant.

Page 4, line 27, please replace the paragraph beginning "Fig. 2 shows an example" with the following:

FIG. 2 shows an example of embodiment of a multilayer stack according to the present invention, which is made up of a number of dielectric layers 10, 12, 14, 16, 18, where the dielectric layer 14 on a ground electrode 30 has a dielectric constant .epsilon..sub.medium which is greater, for example by a factor of 2, than the dielectric constants of the surrounding layers 12, 16. The thickness d_{medium} of the dielectric layer 14

is smaller than that of the surrounding dielectric layers 12, 16 and, in order to keep the interaction with surrounding structures low, the layer thickness d.sub.medium should advantageously be small compared to the distances to adjacent structures, while ε_{medium} on the other hand should be as great as possible. It is thus possible for capacitors having sufficiently small dimensions to be integrated. A metallization structure 20 is arranged at the interface between the dielectric layer 14 and the dielectric layer 12, said metallization structure being composed of a capacitor electrode 22 and a line 24 that partially surrounds the latter. In the particular embodiment illustrated in FIG. 2, for the layer 14, $d_{medium} = 25\mu m$, and $\varepsilon_{medium} = 20$. (Also in the particular embodiment illustrated in FIG. 5a, for the layer 14, $d_{medium} = 25\mu m$, and $\varepsilon_{medium} = 20$.) For adjoining layers 10, 12, 16 and 18 above and below, $d = 100\mu m$ and $\varepsilon = 10$.

Page 5, line 10, please replace the paragraph beginning "The electrical response" with the following:

The electrical response of the circuit according to the invention has great stability with respect to interaction with other metallizations which are located in the multilayer stack above and below the series resonant circuit. In the multilayer stack of ~~FIG. 3~~FIG. 2, above the dielectric layer 12 there is no ground electrode above the metallization structure 20. FIG. 5(a) shows the design of this structure with an additional ground electrode 32 above the metallization structure 20; FIG. 5(b) shows the transmission characteristic, where without a ground electrode (curve I) and at different distances of the additional ground electrode of 100 .mu.m (curve II) and 200 .mu.m (curve III) practically

no variations in the resonant frequency can be seen. This effect is based on the high degree of coupling of the structure according to the invention to the ground electrode 30 arranged at a small distance and the advantageously relatively high dielectric constant compared to that of the surrounding layers.